

Notice of Allowability

Application No.

10/722,193

Examiner

Brook Kebede

Applicant(s)

LEE ET AL.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed on February 15, 2006.
2. ☒ The allowed claim(s) is/are 14-16 and 18-27.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some* c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date ____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date ____
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other ____.

Brook Kebede

BROOK KEBEDE
PRIMARY EXAMINER

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Robert N. Crouse on March 1, 2006.

2. The application has been amended as follows:

In the Claims:

Change claim 14 to --A method of fabricating an integrated circuit device, comprising: **forming a mask layer exposing a predetermined region of a substrate; etching the predetermined region through the mask layer to form at least one shallow trench in the substrate; forming a passivation layer comprising epitaxial silicon-germanium in the shallow trench; removing the mask layer; forming a channel silicon layer on the substrate and on the passivation layer; patterning the channel silicon layer and the substrate to expose sides of the passivation layer and to form a trench defining an active region; selectively removing the exposed passivation layer to form a vacant space; forming a buried insulation layer in the vacant space and forming a field isolation layer in the trench.--.**

Change claim 25 to --A method of fabricating an integrated circuit device, comprising: forming at least one passivation layer **comprising epitaxially grown silicon-germanium in a**

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predetermined region of an integrated circuit substrate **comprising: forming a mask layer; exposing the predetermined region in the substrate; etching the exposed region through the mask layer to form at least one shallow trench in the substrate; forming the passivation layer in the shallow trench; removing the mask layer;** forming a channel silicon layer on the substrate and on the passivation layer; patterning the channel silicon layer and the substrate to expose sides of the passivation layer and to form a trench defining an active region; selectively removing the exposed passivation layer to form a vacant space; forming a buried insulation layer in the vacant space and forming a field isolation layer in the trench; **forming a groove exposing top sides of the active region at a boundary between the field isolation layer and the active region;** forming a gate electrode on the active region and the field isolation layer **so that the gate electrode fills the groove;** forming impurity diffusion layers in the active regions on both sides of the gate electrode to provide a source and a drain region, wherein at least one of the source and drain regions is on the buried insulation layer.--.

Allowable Subject Matter

3. Claims 14-16 and 18-27 are allowed over prior art of record.

Reasons for Allowance

4. The following is an examiner's statement of reasons for allowance:

The prior art of record neither anticipates nor renders obvious the claimed subject matter of the instant application as a whole either taken alone or in combination, in particular, prior art of record does not teach "forming a passivation layer comprising epitaxial silicon-germanium in the shallow trench; removing the mask layer; forming a channel silicon layer on the substrate and on the passivation layer; patterning the channel silicon layer and the substrate to expose sides of

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the passivation layer and to form a trench defining an active region; selectively removing the exposed passivation layer to form a vacant space; forming a buried insulation layer in the vacant space and forming a field isolation layer in the trench,” as recited in claim 14 and “forming the passivation layer in the shallow trench; removing the mask layer; forming a channel silicon layer on the substrate and on the passivation layer; patterning the channel silicon layer and the substrate to expose sides of the passivation layer and to form a trench defining an active region; selectively removing the exposed passivation layer to form a vacant space; forming a buried insulation layer in the vacant space and forming a field isolation layer in the trench; forming a groove exposing top sides of the active region at a boundary between the field isolation layer and the active region; forming a gate electrode on the active region and the field isolation layer so that the gate electrode fills the groove,” as recited in claim 25 respectively.

Claims 15, 16, 18-24, 26 and 27 are also allowed as being directly or indirectly dependent of the allowed independent bas claim.

Conclusion

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

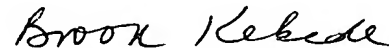
Correspondence

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Brook Kebede
Primary Examiner
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BK
March 4, 2006